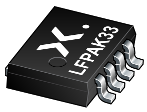

PSMN072-100MSE

N-channel 100 V, 76 mOhm standard level ASFET with enhanced SOA in LFPAK33 package. Recommended for fault tolerant applications including high power PoE, inrush management, eFuse and relay replacement

2 October 2023 Objective data sheet

1. General description

New standards and proprietary approaches are enabling Power-over-Ethernet (PoE) systems capable of delivering up to 90 W to each powered device (PD). Such solutions place increased demands on the power sourcing equipment (PSE) in terms of "soft-start", thermal management and power density requirements. These ASFETs combine enhanced SOA in a compact 3.3 mm x 3.3 mm footprint making them ideally placed for a variety of applications including HP-PoE, eFuse and relay replacement.

2. Features and benefits

- Enhanced safe operating area (SOA) for superior linear mode operation
- Low R_{DSon} for low I^2R losses
- Ultra reliable LFPAK33 package for superior thermal and ruggedness performance
- Very low I_{DSS} leakage

3. Applications

- PoE applications
- IEEE802.3at and proprietary PoE solutions
- Fault tolerant load switch - inrush management and eFuse applications
- Battery management applications
- Relay replacement
- WIFI hotspots
- 5G picocells
- CCTV

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	100	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	-	16	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	45	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C		-	58	76	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 100 °C		-	91	116	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C		[tbd]	0.9	[tbd]	nC
$Q_{G(tot)}$	total gate charge			[tbd]	4.9	[tbd]	nC

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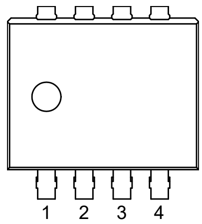
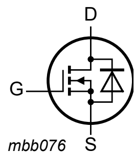
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 9 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 13.4 µs	[1]	-	-	7.8	mJ
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; T_j = 25 °C; Fig. 6		-	21	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK33 (SOT1210)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN072-100MSE	LFPAK33	Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN072-100MSE	72ES10

8. Limiting values

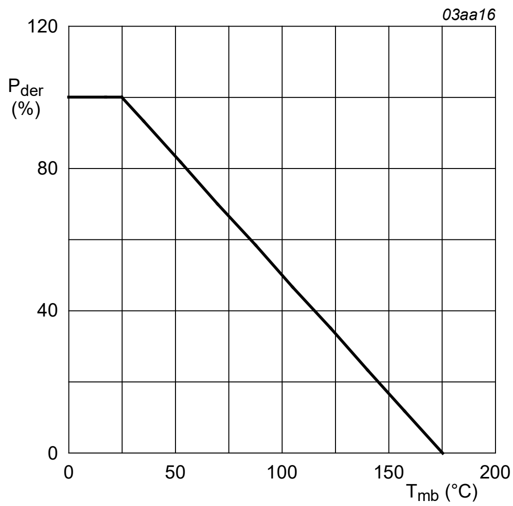
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	100	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	100	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	45	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	16	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	11	A

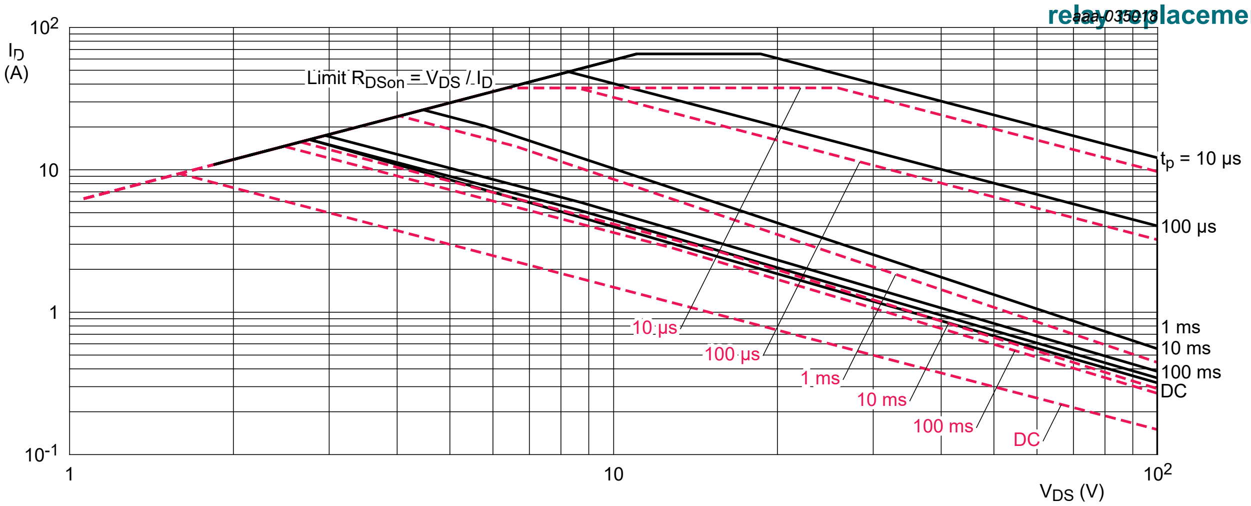
Symbol	Parameter	Conditions		Min	Max	Unit
I_{DM}	peak drain current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C; Fig. 2		-	65	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	16	A
I_{SM}	peak source current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C		-	65	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 9 A; $V_{sup} \leq$ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 13.4 µs	[1]	-	7.8	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} = 100 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω	[1]	-	9	A

[1] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



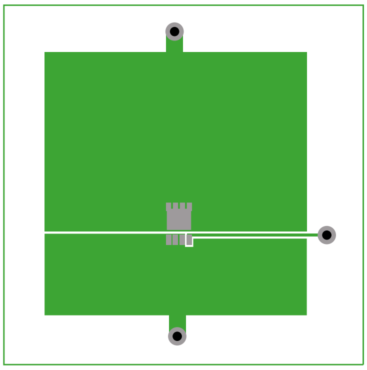
T_{mb} = 25 °C (solid black line); T_{mb} = 125 °C (red dashed line); I_{DM} is a single pulse

Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

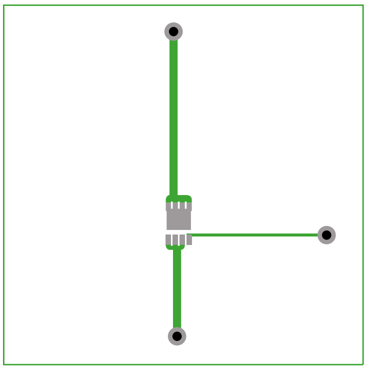
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	[tbd]	3.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 3		-	50	-	K/W
		Fig. 4		-	130	-	K/W



Copper area 25.4 mm x 25.4 mm; 70 µm thick on FR4 board

Fig. 3. PCB layout for thermal resistance from junction to ambient



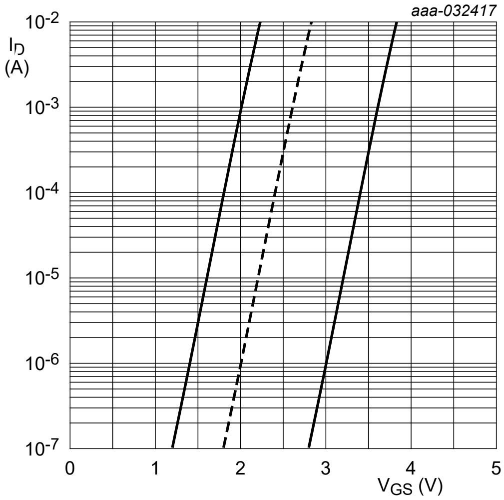
70 µm thick copper on FR4 board

Fig. 4. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 5		2	2.6	3.6	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		-	[tbd]	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	[tbd]	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	[tbd]	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	[tbd]	1	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C		-	-	100	µA
I_{GSS}	gate leakage current	V_{DS} = 20 V; T_j = 25 °C		-	2	100	nA
		V_{DS} = -20 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C		-	58	76	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 100 °C		-	91	116	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 175 °C		-	128	172	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		[tbd]	1.2	[tbd]	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C		[tbd]	4.9	[tbd]	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	2.6	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C		[tbd]	1.4	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	0.9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	0.5	-	nC
Q_{GD}	gate-drain charge			[tbd]	0.9	[tbd]	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 50 V; T_j = 25 °C		-	4.5	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C		[tbd]	345	[tbd]	pF
C_{oss}	output capacitance			[tbd]	76	[tbd]	pF
C_{rss}	reverse transfer capacitance			[tbd]	2.4	[tbd]	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	1.2	-	ns
t_r	rise time			-	1	-	ns
$t_{d(off)}$	turn-off delay time			-	3	-	ns
t_f	fall time			-	1.5	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C		-	-	1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; Fig. 6		-	30	-	ns
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; T_j = 25 °C; Fig. 6		-	21	-	nC



T_j = 25 °C; V_{DS} = 5 V

Fig. 5. Sub-threshold drain current as a function of gate-source voltage

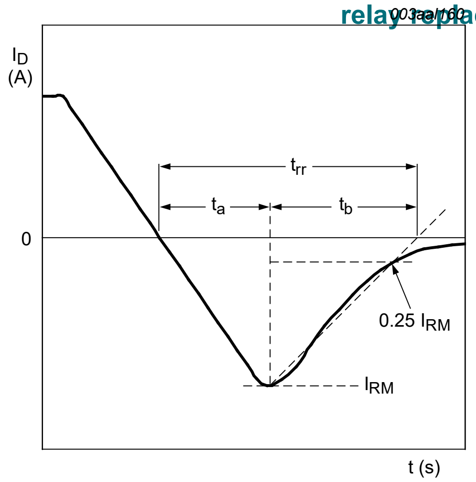
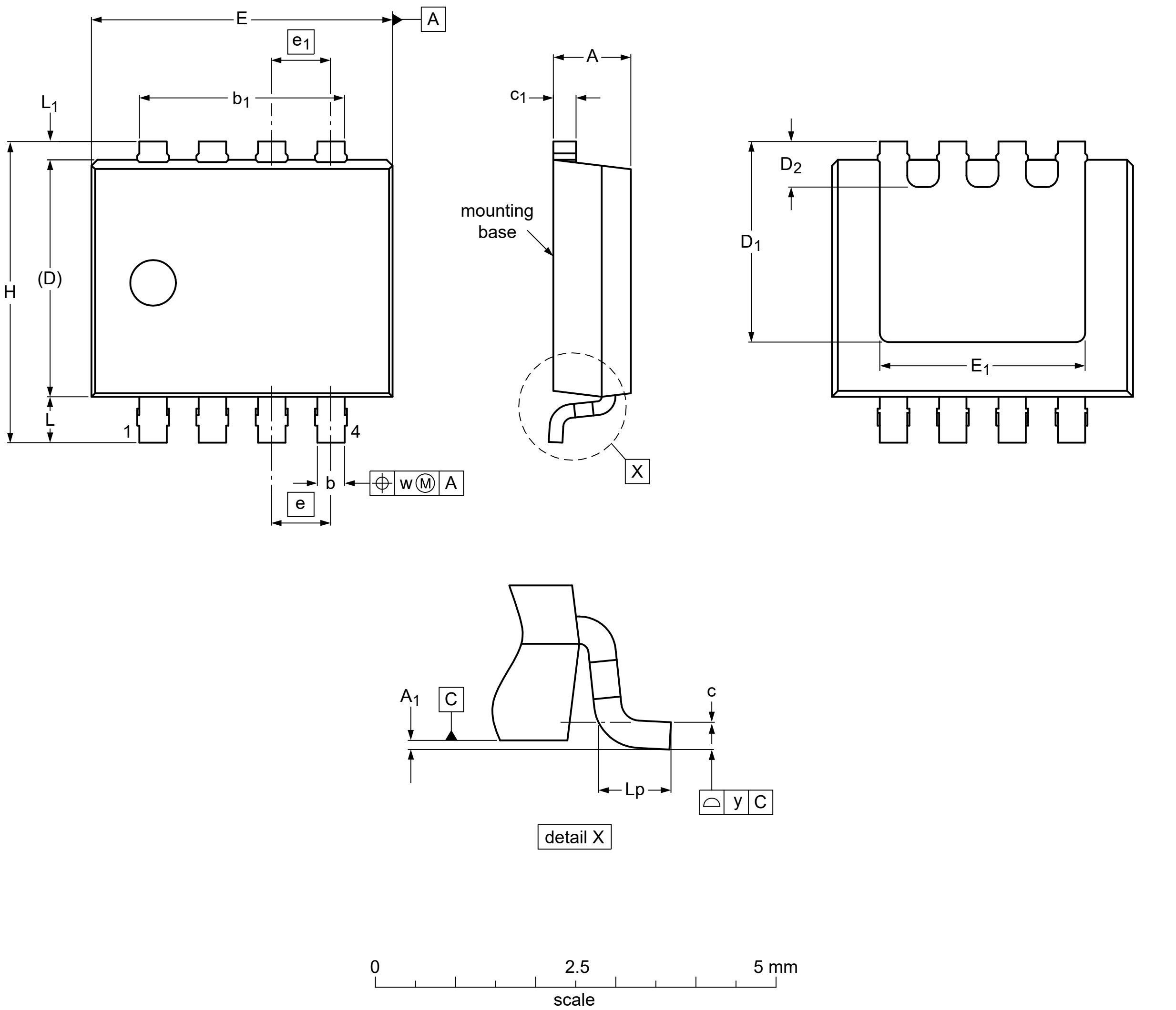


Fig. 6. Reverse recovery timing definition

11. Package outline

Plastic single ended surface mounted package (LFPAK33); 8 leads **SOT1210**



Dimensions

Unit(1)	A	A_1	b(1)	b_1(1)	c	c_1	D ref	D_1	D_2	E(1)	E_1	e	e_1	H	L	L_1	L_p	w	y
mm max	0.90	0.10	0.35	2.4	0.20	0.30		2.35		3.40	2.45			3.40	0.65	0.25	0.50		
mm nom							2.60		0.50			0.65	0.65					0.20	0.10
mm min	0.80	0.00	0.25	2.2	0.10	0.20		1.90		3.20	2.00			3.20	0.45	0.13	0.30		

Note

1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1210_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1210						~~14-04-25~~ 16-08-09

Fig. 7. Package outline LFPAK33 (SOT1210)

12. Soldering

Footprint information for reflow soldering of LFPAK33 package **SOT1210**

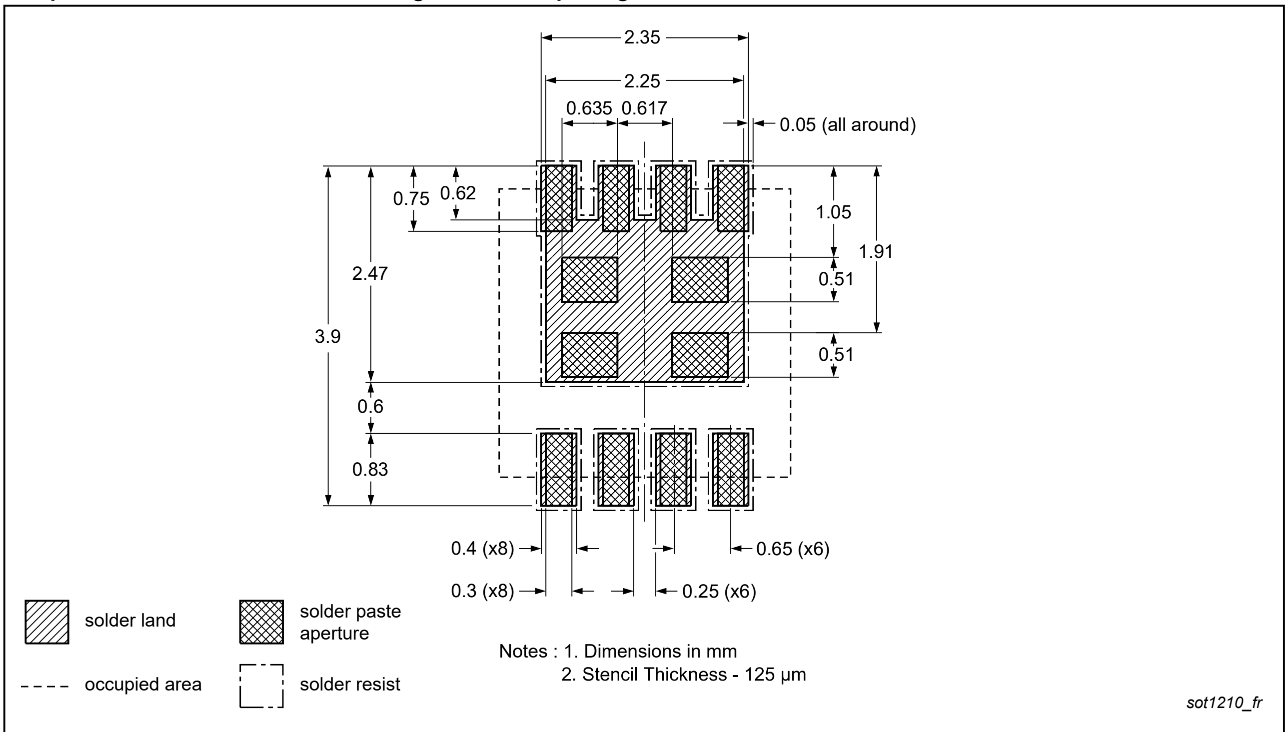


Fig. 8. Reflow soldering footprint for LFPAK33 (SOT1210)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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